

**Amendments to the Drawings:**

Please replace Sheet 1/3 with the attached Replacement Sheet. The Replacement Sheet includes the legend "Prior Art," as requested by the Patent Office.

## REMARKS

This paper is filed in response to the Examiner's non-final Office Action dated August 22, 2007 for the above-captioned U.S. Patent Application.

In the outstanding Action, Figure 1 is objected to as lacking a "Prior Art" legend. Accordingly, Applicant attaches a Replacement Sheet for Figure 1 including the requested Prior Art legend. The objection to the Drawings should therefore be reconsidered and withdrawn.

Regarding the rejection of the claims, claims 1-3, 5, 7 and 9-36 are rejected under 35 USC Section 102(b) as being anticipated by Sevalia et al. (US 6,356,122).

The foregoing rejection is respectfully disagreed with, and is traversed below.

Embodiments of the invention relate to a mechanism for bringing the output signal of a phase locked loop back to the steady state after a change is made to either or both of the counter parameter M of the reference counter or the counter parameter N of the loop counter. This is achieved through the use of a discrete coarse delay and an analogue fine delay. Rather than introducing a single large continuously variable time delay, a discrete delay can be introduced via the reference counter or the loop counter by changing the counter value m or n. The discrete delay is then augmented by a smaller continuously variable delay. This provides the advantage that it enables the delay range of the continuously variable delay component to be reduced and the sensitivity limited.

Claim 1 as amended relates to a phase locked loop circuit for providing an oscillating output signal. The phase locked loop comprises delay circuitry, including a feedback loop, arranged to introduce, in response to a change in the output frequency, a discrete coarse delay into a phase of an input signal provided to the phase detector, and an analogue fine delay into the phase of the input signal wherein the coarse delay and the fine delay effect phase compensation of the input signal.

Independent claim 12 relates to a corresponding method. Claim 15 relates to a frequency synthesizer. Claim 25 is similar to claim 1 except that claim 25 requires that the delay is only added to the first input signal and claim 26 is an

independent method claim corresponding to claim 25. Independent claims 27 and 32 both relate to a frequency synthesizer comprising frequency compensation means having a first input signal and a second input signal. In claim 27 the delays are added to the first signal and in claim 32 the delays are added to the second signal.

In contrast, Sevalia does not disclose or suggest Applicant's claims.

In particular, Sevalia discloses a circuit comprising an oscillator, a reference path, and a feedback path. The oscillator has a reference input receiving a reference signal and a feedback input for receiving the feedback signal. Programmable delay circuits may be included in one or both of these paths in order to compensate for the sources of the delay around the circuit. The delay circuits are user programmable. One of the delay circuits may introduce a coarse delay and the other delay circuit may introduce a fine tuning delay (column 4, lines 5-20).

Sevalia relates to a different technological problem than that of the invention. As mentioned above, the invention provides a mechanism for returning a phase locked loop to the steady state as quickly as possible after a programmed change in the output frequency. Sevalia does not disclose delays being introduced in response to changes in the output frequency, Sevalia is only concerned with including user programmable delays to compensate for the intrinsic delays of components within the circuit.

Sevalia does not teach or suggest any method of returning a phase locked loop back to the steady state after a programmed change in the output frequency. Therefore, there would be no reason why a person skilled in the art would even consider the teachings of Sevalia.

Even if the person skilled in the art did consider the teachings of Sevalia, the result could not be the claimed invention because Sevalia does not teach or suggest the delays being added to the same signal and augmenting each other as indicated by the amended claims. Sevalia teaches that it is advantageous that the programmable delays have opposite effects. Therefore, Sevalia teaches against the delays being added to compensate the same input signal. Accordingly, the Applicant maintains that the invention is new and non-obvious with respect to Sevalia.

In view of the foregoing, all claims are believed to patentably distinguish over the cited art. Accordingly, reconsideration and withdrawal of the outstanding rejection is requested. The Applicant respectfully requests the Examiner to pass pending claims 1-36 to issue. The undersigned representative also welcomes the opportunity to resolve any matters that may remain, formal or otherwise, via teleconference at the Examiner's convenience.

Respectfully submitted:

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11/21/07  
Date

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

11-21-07  
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